

DSMO No.: M4065.0374/P374
Micron No.: 99-1057

**IN THE UNITED STATES PATENT AND TRADEMARK
OFFICE APPLICATION FOR U.S. LETTERS PATENT**

**SEMICONDUCTOR ASSEMBLY WITHOUT
ADHESIVE FILLETS**

Inventor:

Jerry M. Brooks

Dickstein Shapiro Morin
& Oshinsky LLP
2101 L Street NW
Washington, DC
20037-1526
(202) 785-9700

FIELD OF THE INVENTION

The present invention relates to a structure and method of forming a semiconductor assembly using adhesive materials to secure semiconductor dies to support elements without forming adhesive fillets.

5

BACKGROUND OF THE INVENTION

In order to reduce the size of semiconductor devices numerous techniques have been developed to vertically stack one semiconductor die, hereinafter "die", on top of another die. Figure 1 illustrates a conventional method of vertically stacking two die 20, 30 on a support

10 structure 10, such as a printed circuit board (PCB) or other thin support structure, to form a conventional semiconductor assembly 100. The first die 20 is shown secured to a support structure 10 by an adhesive material 22 using techniques well known in the art. When the first die 20 is pressed against the support structure 10 the adhesive material 22 is 15 partially forced outside the die's perimeter 29 and forms an adhesive fillet 24. Likewise, when the second die 30 is secured against the first die 20 by an adhesive material 22 a second adhesive fillet 24 is also formed.

Both the first die 20 and second die 30 are shown wire bonded 40 to an electrical contact area 18 on the support structure 10. The first die 20 has an electrical contact area 28, such as a bonding pad, on its top

surface 26. Because adhesive fillet 24 is formed when the second die 30 is secured to the first die 20, it limits the placement of the first die's 20 electrical contact area 28. The distance B between the perimeter 39 of the second die 30 and the first die's electrical contact area 28 must be increased by distance A, the width of the adhesive fillet 24, to provide sufficient operating space for the wire bonding equipment. Typical dimensions for distances B are about 428 microns or greater to allow for adhesive fillets 24, which are conventionally about 228 microns in width or greater. Using current wire bonding equipment, distance B between 10 electrical contact area 28 and the perimeter of the fillet 24 can be reduced to about 200 microns or less. In other words, adhesive fillet 24 requires about 228 microns or more of first die's top surface 26 on each side of the first die 20. If the adhesive fillet 24 were eliminated the space could be used either to increase the size of the second die 30 or to reduce the 15 size of the first die 20.

An alternative method of stacking dies 20, 30 to a support structure 10 to form a semiconductor assembly involves using an adhesive film sized and aligned with the respective die 20, 30 perimeters. Since the adhesive film is cut or dimensioned with the second die's perimeter 39, no adhesive fillet 24, as described above, is formed. However, adhesive films 20 are expensive and are difficult to align with the dies 20, 30 and support

structure 10. Accordingly, there is a need and desire for an easy, low-cost method of securing one or more semiconductor dies 20, 30 to various support structures 10 to form a semiconductor assembly 100 using adhesive materials 22 such that no adhesive fillets 24 are produced, for example, when a second die 30 is pressed and secured to a first semiconductor die 20 and when a first semiconductor die 20 is pressed and secured to a support structure 10.

SUMMARY OF THE INVENTION

The present invention provides a method to vertically stack at least one semiconductor die on top of another semiconductor die using an adhesive material without forming an adhesive fillet at the second die's perimeter. An adhesive material is deposited over about 50% to about 90% of the top surface of the first semiconductor die, such that when the second die is secured against the adhesive material and first die no adhesive material extends past the perimeter of the second die. Because no adhesive fillet is formed, the distance between the electrical contact areas on top of the first semiconductor die and the perimeter of the second die can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages and features of the invention will become more apparent from the detailed description of the preferred embodiments given below with reference to the accompanying drawings
5 in which:

Figure 1 is an illustration of a conventional structure in which two stacked semiconductor die are secured to a support structure by an adhesive material;

10 Figure 2 is a plan view of a partially fabricated semiconductor die stack on a support structure according to the present invention;

Figure 3 is an elevation view of Figure 2;

Figure 4 is a plan view of a partially fabricated semiconductor die stack at a stage of processing subsequent to that shown in Figures 2 and 3;

Figure 5 is an elevation view of Figure 4;

15 Figure 6 is a cross-sectional illustration of an encapsulated semiconductor die stack formed according to a method of the present invention; and

Figure 7 is an exemplary embodiment of two semiconductor dies stacked on top of a semiconductor die according to a method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 The invention provides a method and resulting structure for a semiconductor assembly with no adhesive fillet formed when a semiconductor die is secured by adhesive to a supporting structure. The invention will be described as set forth in the exemplary embodiments of the detailed description and as illustrated in Figures 2-7. These 10 embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural changes may be made without departing from the spirit or scope of the invention. The invention is not limited by the description of the exemplary embodiments.

15 Referring now to the drawings, where like elements are designated by like reference numerals, Figures 2-3, illustrate a plan and elevation view respectively of a partially completed semiconductor assembly 200 in which a first semiconductor die 20 is secured to the top surface 16 of supporting structure 10, by a first adhesive layer 22. Supporting structure 10 in an exemplary embodiment is a printed circuit board or thin film, but may be 20 any structure suitable for supporting a semiconductor die. The

supporting structure 10 is shown as having two electrical contact areas 17 on surface 16 and the first die 20 is also shown as having two electrical contact areas 28. It is to be understood that any number of electrical contact areas 17, 28 may be provided on the support structure 10 and first die 20. Also, although Figure 2 shows the contact areas 17, 28 as recessed, they may also be formed on the surface of the support structure 10 or first die 20, respectively, and could be electrically connected to external electrical paths or to other parts of the completed semiconductor assembly 200.

10 A second adhesive layer 22 is shown in Figure 2 as deposited on the top surface 26 of the first semiconductor die 20 within an adhesive layer area defined by a perimeter 34. The second adhesive layer 22 can be deposited by techniques well-known in the art to include various patterns and coverage areas. It is to be understood that perimeter 34 is representative of an area of deposition of the second adhesive layer 22; however it is not limiting. In accordance with the invention a sufficient amount of adhesive material 22 should be deposited to adequately secure the second semiconductor die 30 (see Figures 4-5) to the first semiconductor die 20. The invention includes any coverage area or pattern that does not exceed the perimeter of the second die 30. As described below, when the second die 30 is placed and pressed on the first

die 20, the adhesive layer 22 represented inside of the adhesive perimeter 34 does not extend past the profile or perimeter 39 of the second die 30 (Figures 4-5).

Figures 4-5 show the assembly 200 after a second die 30 with 5 electrical contact areas 38 on the die's top surface 36 is pressed against the second adhesive layer 22 located on the top surface 26 of the first die 20. A cavity 24 is formed between the dies 20 and 30 and is characterized by a distance D between the perimeter 34 of the second adhesive layer 22 and the perimeter 39 of the second die 30. The distance D may be a 10 regular or irregular distance around the periphery of the adhesive layer 22. It is to be understood that formation of cavity 24 is not essential, what is important is that adhesive layer 22 does not extend beyond the perimeter 39 of the second die 30 such that no adhesive fillet 24 is formed.

If cavity 24 is present, the distance D is preferably in the range 15 such that between about 50 and about 90 percent of the second die 30 bottom surface is covered by the second adhesive material layer 22.

Figures 4 and 5 show distance C between the perimeter 39 of the second die 30 and the perimeter 29 of the first die 20. This distance is a value 20 which provides acceptable clearance between electrical contact area 28 and the second die 30 to enable the formation of electrical contacts between the dies 20, 30 and other parts of the assembly 20 such as wire

bonds 40 between the dies 20, 30 and the support structure 10 (Figures 6). An exemplary distance C between the perimeters 29, 39 of the first die 20 and second die 30 is about 200 microns or less. The distance C is currently only limited by the technology of the wire bond equipment and 5 the minimum required operating space.

Figure 6 is a cross-sectional illustration of the semiconductor assembly 200 after electrical connections 40 have been made between the respective electrical contact areas 28 and 38 of the first die 20 and second die 30 and electrical contact areas 17 of the support structure 10. In an exemplary embodiment, wire bonding is used for these connections. As 10 illustrated, the dies 20, 30 are stacked and positioned in such a manner that at least one of the electrical contact areas 28, 38 for each die 20, 30 is exposed and accessible for making the electrical connection. Illustrated distance E represents the distance between the first die's electrical contact 15 area 28 and the perimeter 39 of the second die 30.

Also shown are the balls 60 which make up a ball grid array pattern for making electrical connections between the support structure 10 and external electrical circuits. The balls 60 are deposited on the support structure 10 using materials and techniques well known in the art and are 20 electrically connected through conductors supported by support structure 10 to the contact areas 17. It is to be understood that multiple

semiconductor assemblies 200 could be prepared at one time on a continuous support structure 10, which could be separated into individual or multiple semiconductor assemblies 200 at a later stage of fabrication.

Figure 6 also shows an encapsulating material 50, such as a 5 molding compound, deposited over the wire bonds 40, semiconductor dies 20, 30, and top surface 16 of the support structure 10. As an exemplary illustration, some of the encapsulation material 50 is shown under the second die 30 and within cavity 24 (Figures 4-5) and provides support and stability to the second die 30. The encapsulating material 50 10 and molding techniques using it are well known in the art and not repeated herein.

Figure 7 is a cross-sectional illustration of a second exemplary embodiment of a semiconductor assembly 300 with second and third semiconductor dies 30, 40 secured to a first semiconductor die 20 using the techniques described above. It is to be understood that the 15 elimination of the adhesive fillet 24 as discussed in Figure 1 covers a wide range of semiconductor configurations involving multiple dies with various sizes, dimensions, and electrical contact techniques. The above described invention has the advantage of allowing either the size of the 20 second and third semiconductor dies 30, 40 to be increased or allowing

the size of the first semiconductor die 20 to be reduced by eliminating the wasted space occupied by the adhesive fillet 24.

Having thus described in detail the exemplary embodiments of the invention, it is to be understood that the invention defined by the 5 appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof are possible without departing from the spirit or scope of the invention. Accordingly, the above description and accompanying drawings are only illustrative of exemplary embodiments which can achieve the features and advantages of 10 the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the scope of the following claims.